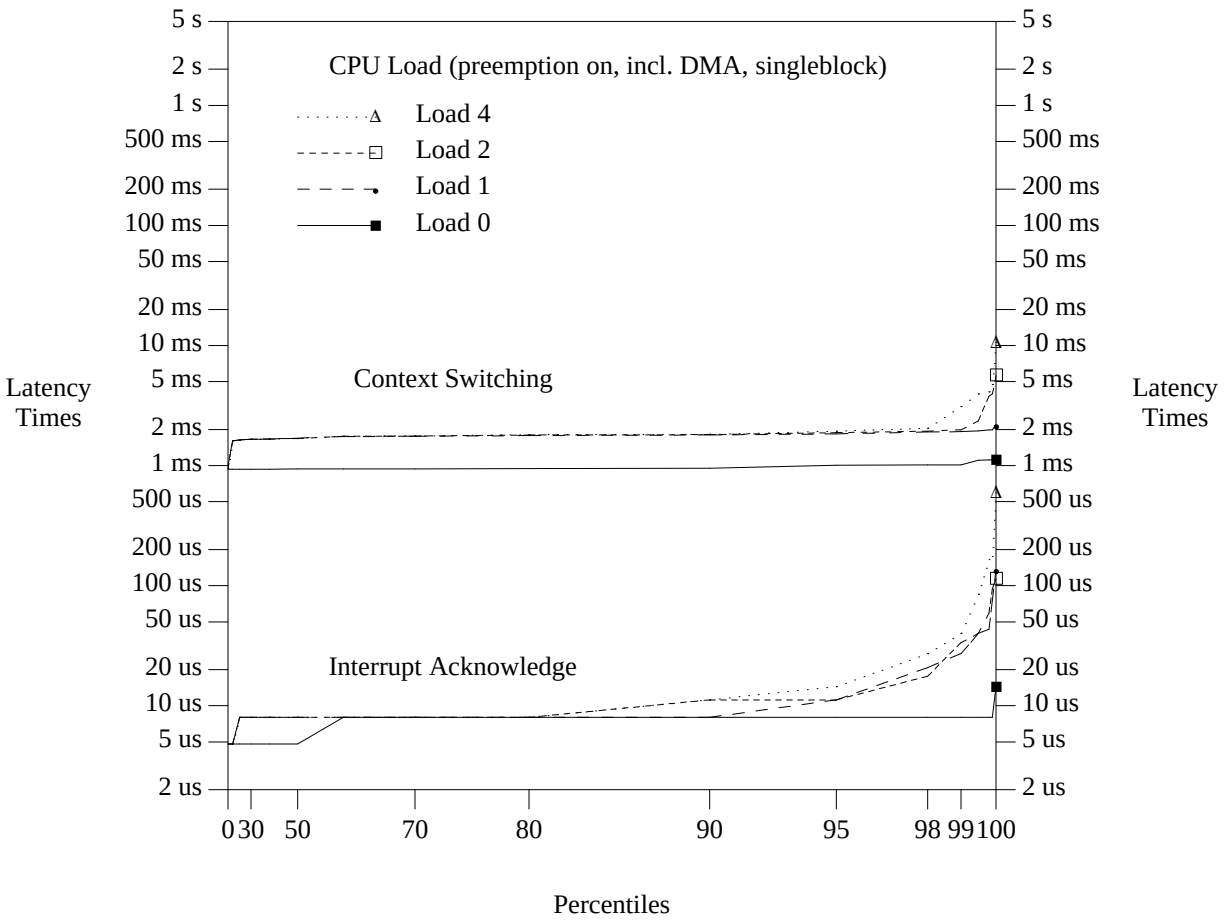

Figure 1

CPU Load (preemption on, incl. DMA, singleblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	14.4	9.89	1.62
load 1	4.8	8.0	136.0	12.13	6.48
load 2	4.8	8.0	113.6	12.23	6.47
load 4	4.8	8.0	593.6	13.59	23.50
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	1694	2184	1704	87
load 2	939	1682	5614	1716	235
load 4	936	1682	10610	1740	431

Table 1

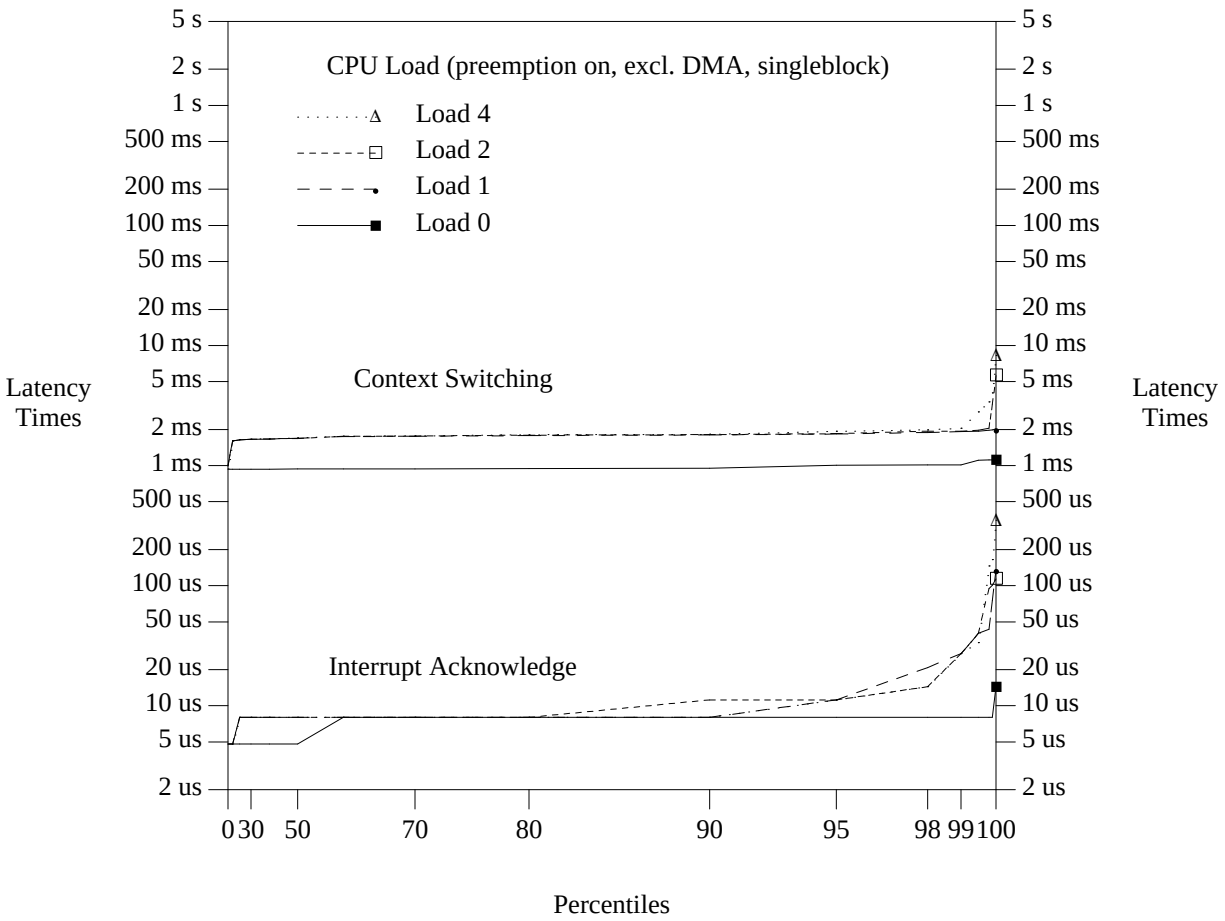

Figure 2

CPU Load (preemption on, excl. DMA, singleblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	14.4	9.89	1.62
load 1	4.8	8.0	136.0	12.10	6.41
load 2	4.8	8.0	113.6	12.13	6.13
load 4	4.8	8.0	350.4	12.59	13.84
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	1691	2018	1704	86
load 2	994	1682	5614	1710	172
load 4	936	1698	8267	1725	274

Table 2

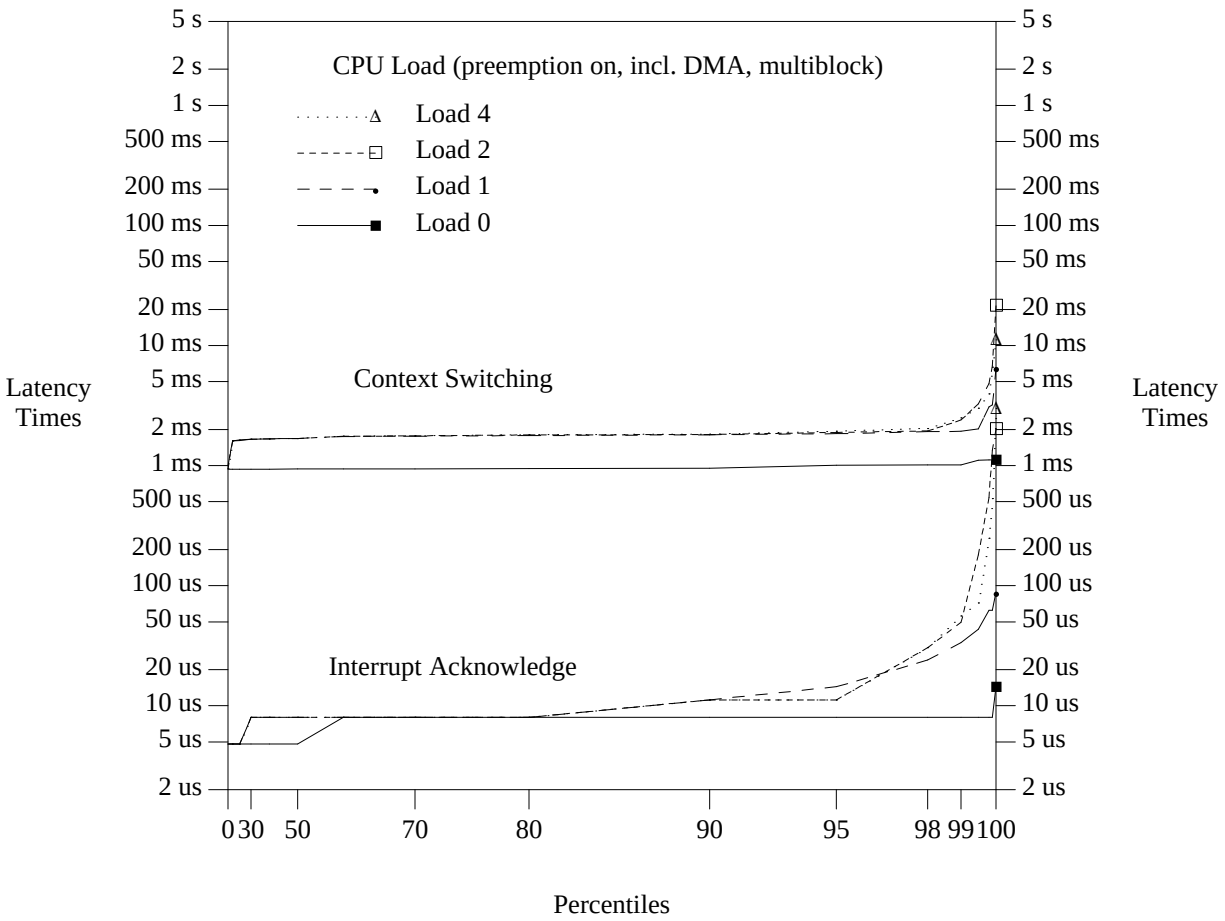

Figure 3

CPU Load (preemption on, incl. DMA, multiblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	14.4	9.89	1.62
load 1	4.8	8.0	88.0	11.94	5.83
load 2	4.8	8.0	2014.4	17.74	90.64
load 4	4.8	8.0	2993.6	16.85	99.96
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	1682	6546	1712	197
load 2	939	1678	21413	1739	712
load 4	942	1682	11176	1737	478

Table 3