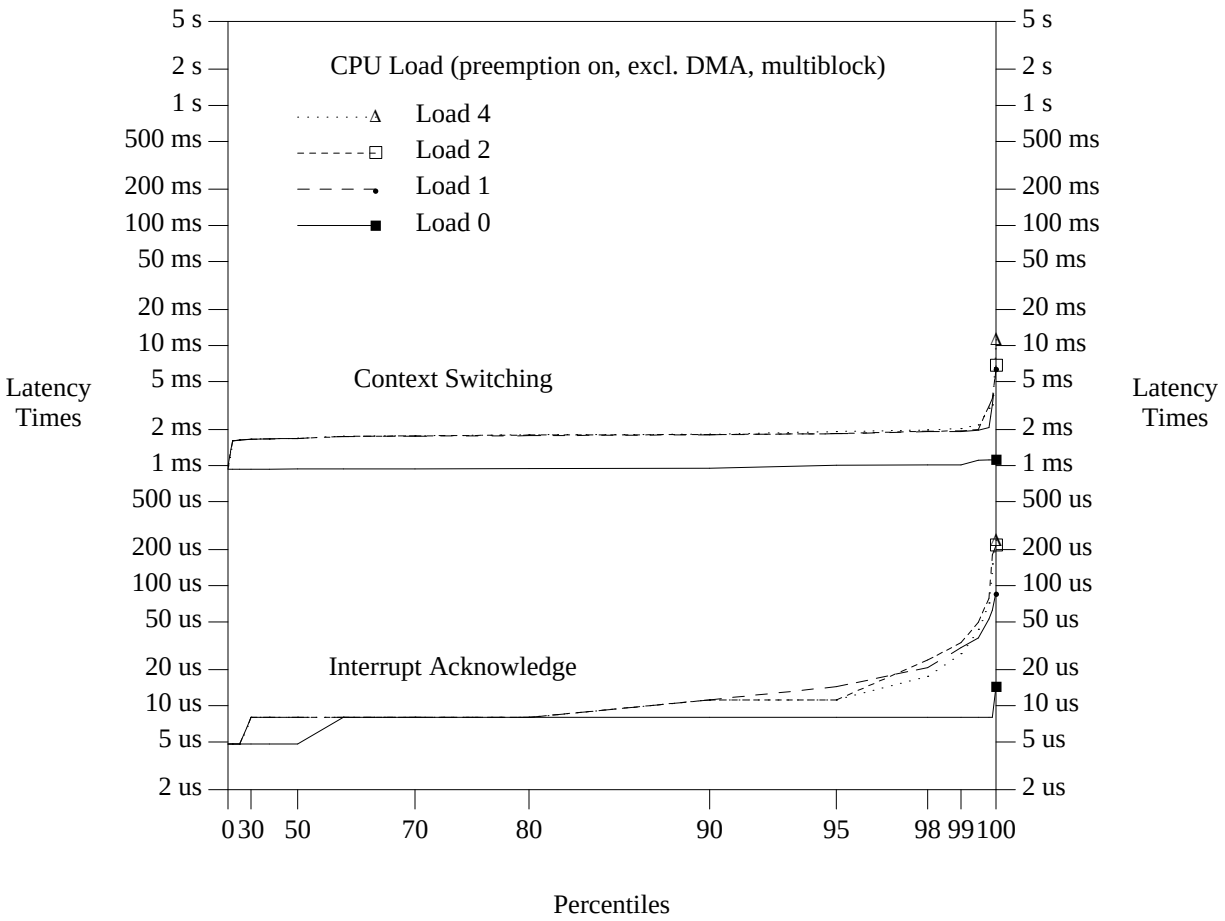

Figure 4

CPU Load (preemption on, excl. DMA, multiblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	14.4	9.89	1.62
load 1	4.8	8.0	88.0	11.89	5.59
load 2	4.8	8.0	216.0	12.18	10.13
load 4	4.8	8.0	238.4	12.00	9.87
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	1682	6546	1710	191
load 2	939	1678	6754	1702	228
load 4	994	1685	11176	1721	344

Table 4

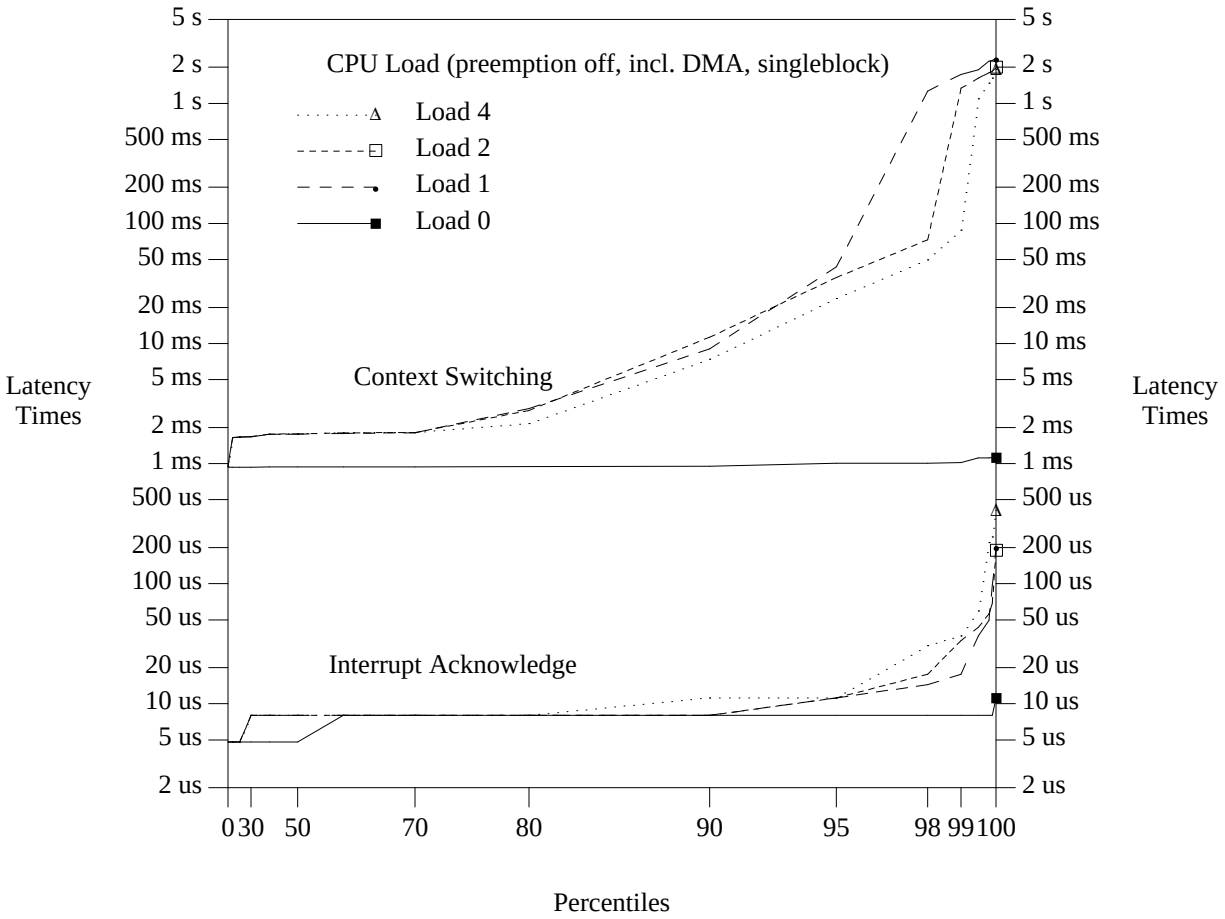

Figure 5

CPU Load (preemption off, incl. DMA, singleblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	11.2	9.92	1.60
load 1	4.8	8.0	203.2	11.70	8.44
load 2	4.8	8.0	187.2	11.68	7.44
load 4	4.8	8.0	408.0	12.93	20.71
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	942	1758	2376561	53826	281996
load 2	946	1768	1974965	29499	191326
load 4	942	1768	1915694	17015	135660

Table 5

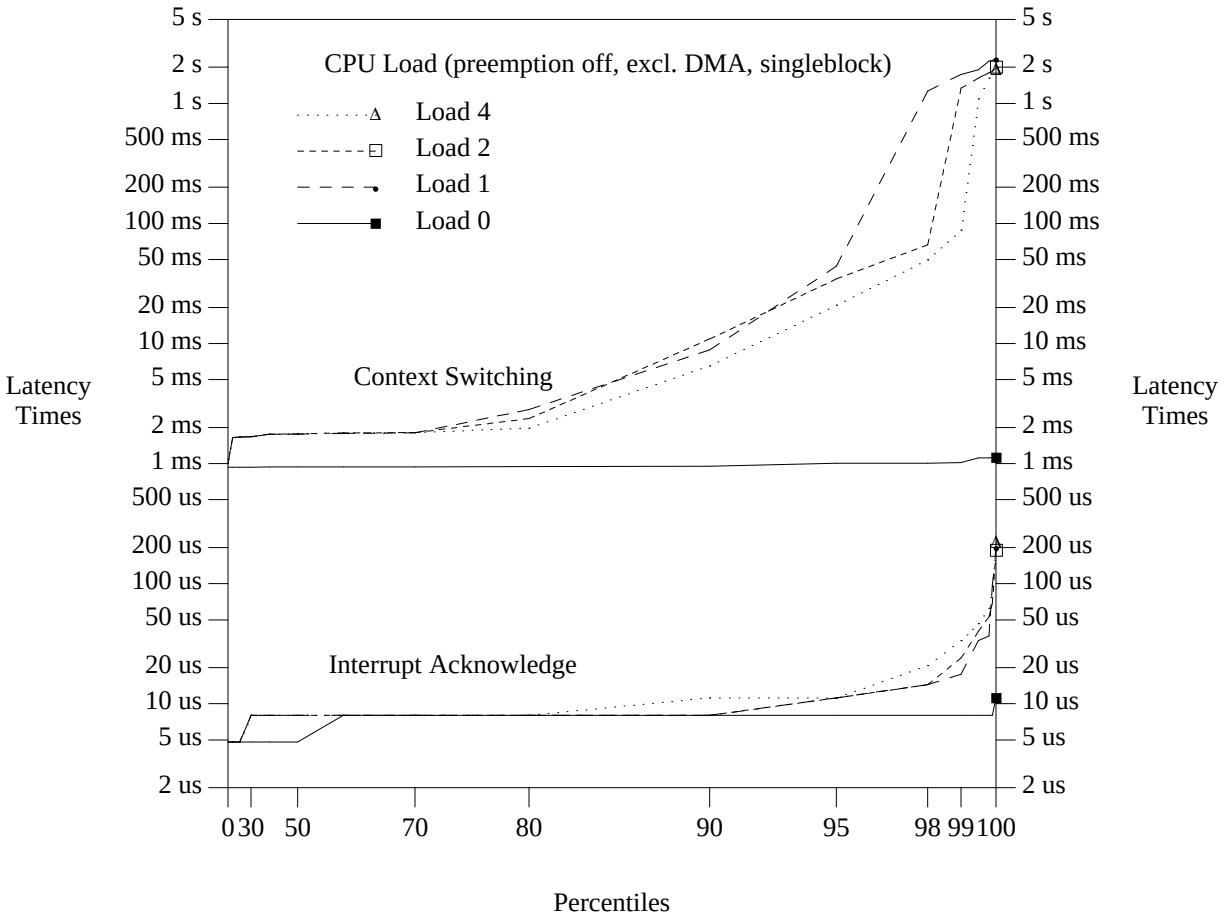

Figure 6

CPU Load (preemption off, excl. DMA, singleblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	11.2	9.92	1.60
load 1	4.8	8.0	203.2	11.68	8.41
load 2	4.8	8.0	187.2	11.59	7.22
load 4	4.8	8.0	219.2	11.93	8.70
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	1758	2376561	54810	284705
load 2	994	1768	1974965	28177	188595
load 4	1090	1768	1915694	16058	131431

Table 6