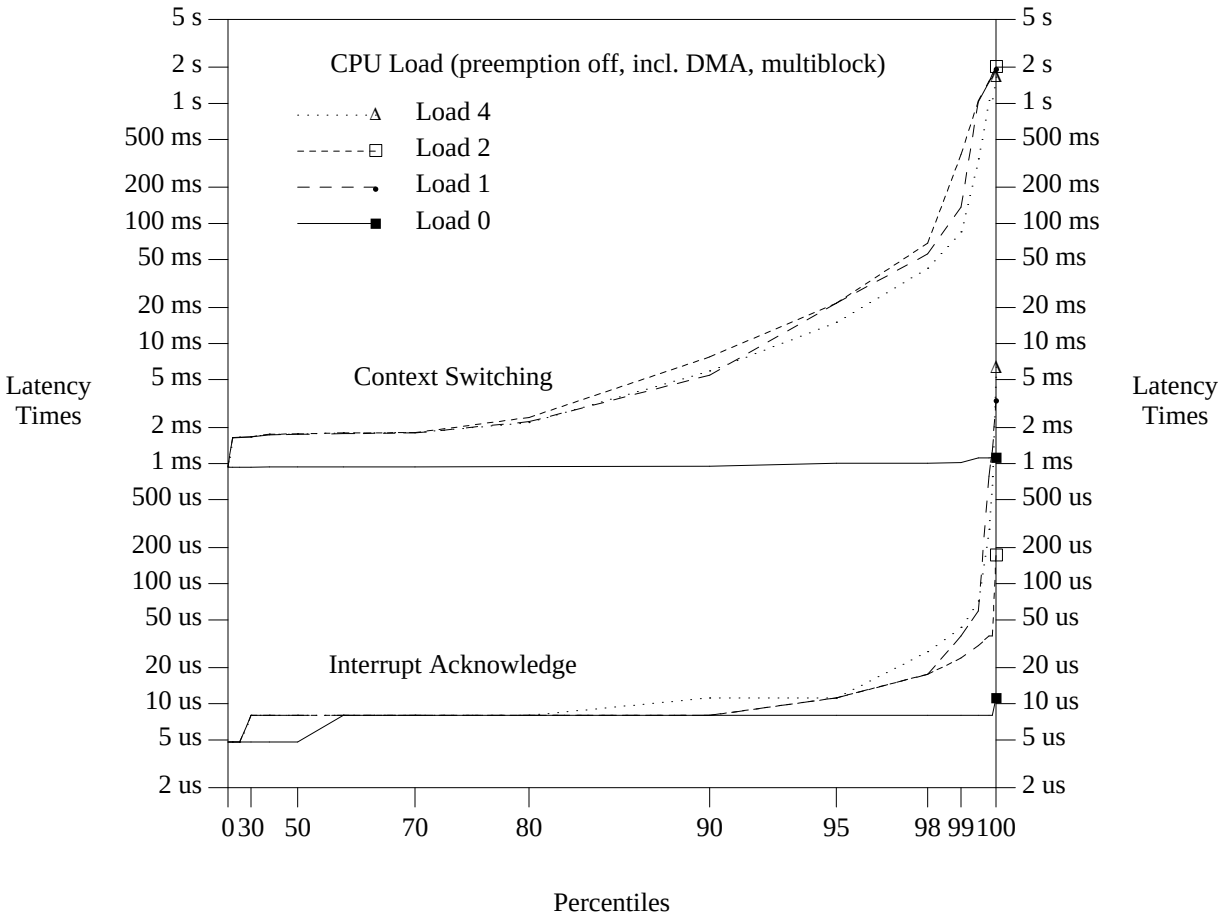

Figure 7

CPU Load (preemption off, incl. DMA, multiblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	11.2	9.92	1.60
load 1	4.8	8.0	3460.8	18.61	125.84
load 2	4.8	8.0	171.2	11.63	6.31
load 4	4.8	8.0	6340.8	22.53	223.85
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	940	1755	1993531	15588	127405
load 2	946	1765	1997550	18056	134663
load 4	940	1765	1657474	11072	90162

Table 7

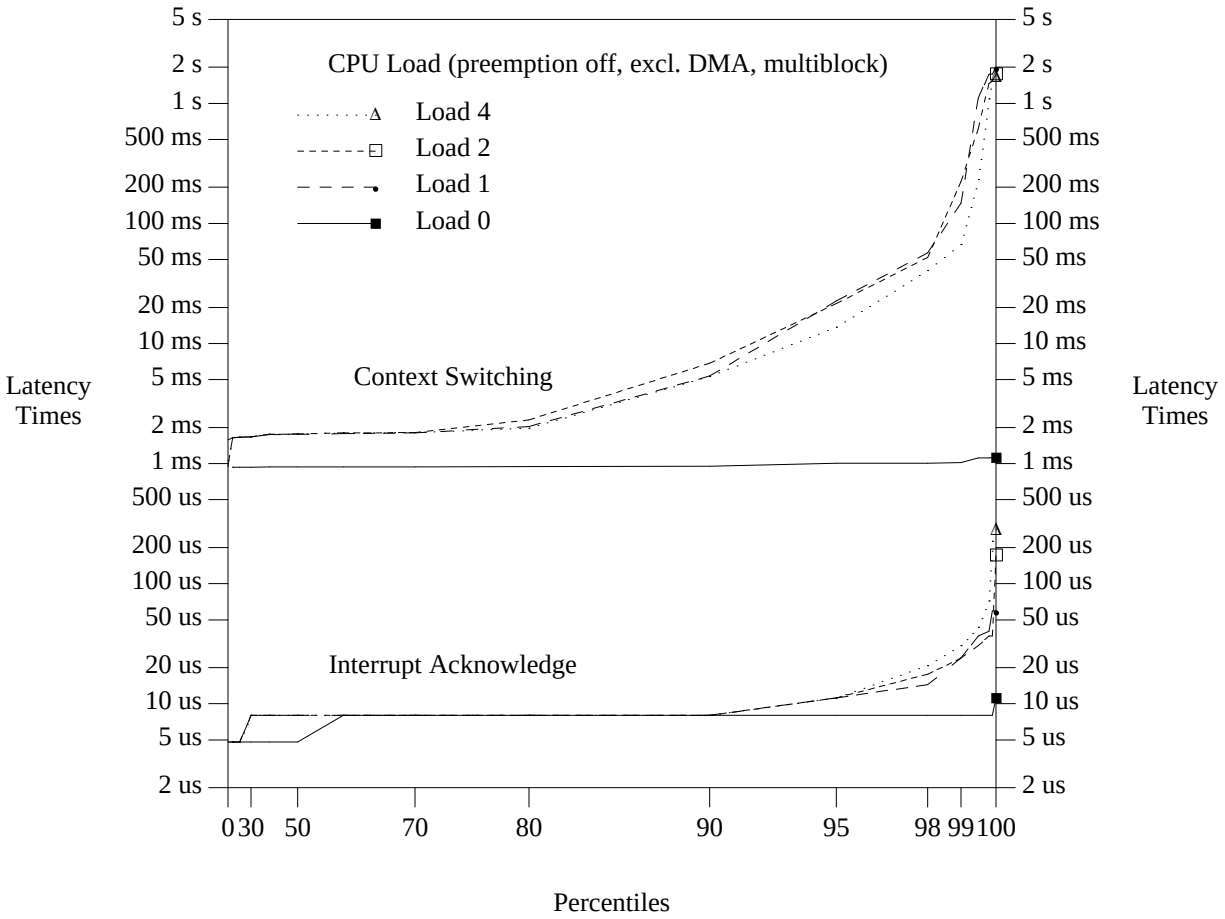

Figure 8

CPU Load (preemption off, excl. DMA, multiblock)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	11.2	9.92	1.60
load 1	4.8	8.0	59.2	11.45	3.94
load 2	4.8	8.0	171.2	11.62	6.33
load 4	4.8	8.0	283.2	12.09	12.06
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	942	1755	1993531	15923	129294
load 2	1576	1765	1745483	15630	118748
load 4	1064	1765	1657474	9329	83273

Table 8

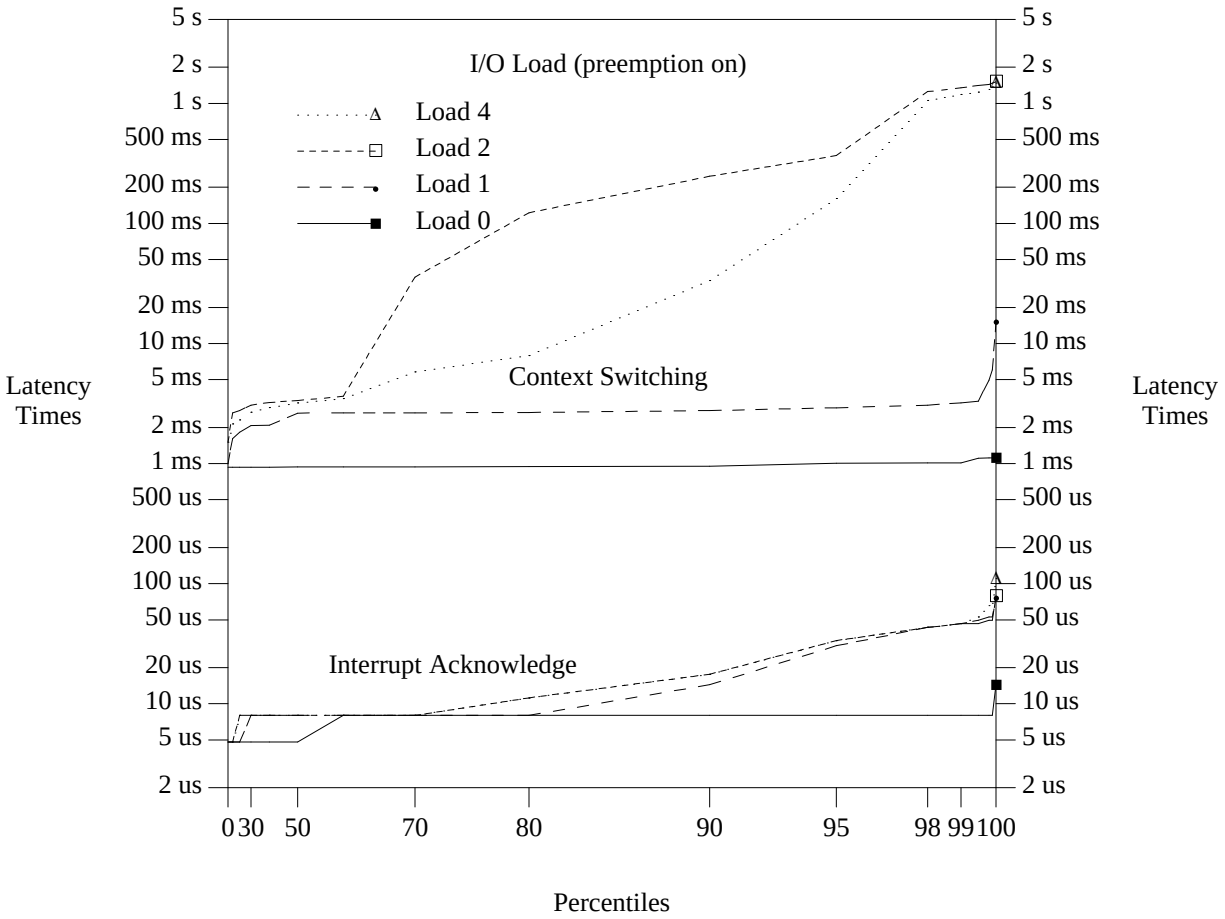

Figure 9

I/O Load (preemption on)					
Interrupt Acknowledge (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	4.8	4.8	14.4	9.89	1.62
load 1	4.8	8.0	78.4	13.40	8.14
load 2	4.8	8.0	78.4	14.38	8.70
load 4	4.8	8.0	110.4	14.55	9.68
Context Switching (microseconds)					
	min.	med.	max.	average	std. dev.
load 0	933	936	1122	943	27
load 1	994	2635	15598	2339	645
load 2	1506	3352	1510565	101503	262710
load 4	1506	3195	1471656	42334	182026

Table 9